UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/646,665	11/27/2000	Masaaki Higashida	MAT-8014US	5725

7590 10/30/2006

Lawrence E Ashery
Ratner & Prestia
One Westlakes Berwyn Suite 301
PO Box 980
Valley Forge, PA 19482-0980

EXAMINER	
MILLS, DONALD L	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/646,665	HIGASHIDA ET AL.	
	Examiner	Art Unit	
	Donald L. Mills	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7 and 12-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,12-15,17-30 and 32-35* is/are rejected.

7)☒ Claim(s) *7,16,31 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 September 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujimoto et al. (US 6,191,903 B1), hereinafter referred to as Fujimoto.

Regarding claims 1 and 14, Fujimoto discloses a recording medium, data transmission apparatus, data receiver and optical disk unit for the transmission of video and other data, which comprises:

Generating (Claim 1)/Means for generating (Claim14) a fixed pattern comprising 'm' words (Note: the Examiner interprets a word as one bit. Referring to Figure 3, bits 0-7 and 8-15.)

Generating (Claim 1)/Means for generating (Claim14) variable, non-random patterns of predetermined bit structure, each pattern comprising 'n' words (Referring to Figure 3, bits 16-23 and 24-31.)

Generating (Claim 1)/Means for generating (Claim14) sync patterns comprising 'q' words, each of the sync patterns formed by combining the fixed pattern and one of the variable patterns (Referring to Figure 3, the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a fixed and variable portion; therefore, comprising different composite patterns. See column 5, lines 33-38.)

Adding one of said sync patterns to each of said data packets in a data stream, wherein consecutive ones of said data packets each have added respectively different variable patterns (Referring to Figures 3 and 4, no identical combination of synchronization patterns occurs among contiguous sync frames. See column 5, lines 45-50.)

Wherein the variable pattern comprises a plurality of words, and the variable patterns are made by changing an order of the words (Referring to Figure 3, the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a variable portion, with different bit patterns, comprised of different composite patterns. See column 5, lines 33-38.)

Regarding claim 12, Fujimoto discloses *the method including a step of detecting a sync* (Referring to Figures 2-4, the memory **8** can locate a sync frame by two contiguous synchronization patterns. See column 5, lines 54-56.)

Regarding claims 13 and 15, Fujimoto discloses:

Detecting (Claim 13)/Means for detecting (Claim 15) a sync for examining both of a fixed pattern and a variable pattern of a data received (Referring to Figures 2 and 3, the synchronization pattern is detected to identify the data packet. See column 7, lines 44-47.)

Securing (Claim 13)/Means for securing (Claim 15) a sync for examining only the fixed pattern (Referring to Figures 2 and 3, during synchronization the synchronization pattern is inherently examined individually in order to determine the value of each bit.)

Wherein step (a) processes the data until the sync is secured and step (b) processes the data after the sync is secured (Referring to Figures 2-4, when correctly detecting contiguous synchronization patterns, the frame number decoder **31** detects a sync frame number equal to the count value of the frame counter **32** and controls the frame counter **32** so as to output a frame number based on the detected number. See column 7, lines 61-65.)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-6, 25-30, and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto et al. (US 6,191,903 B1), hereinafter referred to as Fujimoto.

Regarding claims 3 and 27 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Fujimoto does not disclose *wherein the fixed pattern comprises three words.*

Fujimoto teaches, referring to Figure 3, the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a fixed portion (bits 1-15) comprised of two fixed bytes (words) (See column 5, lines 33-38.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement additional bits in the synchronization pattern Fujimoto. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to provide synchronization in error prone sectors, thereby, providing greater error correction capability.

Regarding claim 4 and 28 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Fujimoto does not disclose *wherein the three words include 'eb', 'cb' and 'aa', expressed in a hexadecimal notation.*

Fujimoto teaches, referring to Figure 3, the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a fixed portion (bits 1-15) comprised of two fixed bytes (words) (See column 5, lines 33-38.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine three different arbitrary fixed patterns in the synchronization pattern of Fujimoto. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to provide synchronization in error prone sectors, thereby, providing greater error correction capability.

Regarding claim 5 and 29 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Fujimoto does not disclose *wherein the variable pattern comprises five words.*

Fujimoto teaches the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a variable portion (bits 16-31), two bytes, comprised of different composite patterns. (See column 5, lines 33-38.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the length of the synchronization pattern to comprise five words in the system of Fujimoto. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to provide synchronization in error prone sectors, thereby, providing greater error correction capability.

Regarding claim 6 and 30 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Fujimoto does not disclose *wherein the five words include '4c', 'ea', 'cd', '7a' and '81', expressed in a hexadecimal notation.*

Fujimoto teaches the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a variable portion (bits 16-31), two bytes, comprised of different composite patterns (See column 5, lines 33-38.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the length of the synchronization pattern to comprise five arbitrary words in the system of Fujimoto. One of ordinary skill in the art at the time of the invention would have been motivated to do so in order to provide synchronization in error prone sectors, thereby, providing greater error correction capability.

Regarding claims 25 and 34, Fujimoto discloses a recording medium, data transmission apparatus, data receiver and optical disk unit for the transmission of video and other data, which comprises:

Generating a fixed pattern comprising 'm' words (Note: the Examiner interprets a word as one bit. Referring to Figure 3, bits 0-7 and 8-15.)

Generating variable, non-random patterns of predetermined bit structure, each pattern comprising 'n' words (Referring to Figure 3, bits 16-23 and 24-31.)

Generating sync patterns comprising 'q' words, each of the sync patterns formed by combining the fixed pattern and one of the variable patterns (Referring to Figure 3, the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a fixed and variable portion; therefore, comprising different composite patterns. See column 5, lines 33-38.)

Adding one of said sync patterns to each of said data packets in a data stream, wherein consecutive ones of said data packets each have added respectively different variable patterns (Referring to Figures 3 and 4, no identical combination of synchronization patterns occurs among contiguous sync frames. See column 5, lines 45-50.)

Fujimoto does not disclose *wherein the variable patterns are two patterns.*

Fujimoto teaches interleaving synchronization patterns to result in unique combinations, comprising eight variable patterns (Referring to Figure 3, see column 5, lines 33-41.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a reduced number of variable patterns, two in particular, in the system of Fujimoto. One of ordinary skill in the art at the time of the invention would have been motivated to do so in

order to efficiently and effectively reduce sector searching time on an optical disk comprising only a few sectors of data as taught by Fujimoto (See column 1, lines 51-55.)

Regarding claim 26, the primary reference further teaches *wherein the variable pattern comprises a plurality of words, and the variable patterns are made by changing an order of the words* (Referring to Figure 3, the synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a variable portion, with different bit patterns, comprised of different composite patterns. See column 5, lines 33-38.)

Regarding claim 32, the primary reference further teaches *the method including a step of detecting a sync* (Referring to Figures 2-4, the memory **8** can locate a sync frame by two contiguous synchronization patterns. See column 5, lines 54-56.)

Regarding claims 33 and 35, the primary reference further teaches comprising:

Detecting/Means for detecting a sync for examining both of a fixed pattern and a variable pattern of a data received (Referring to Figures 2 and 3, the synchronization pattern is detected to identify the data packet. See column 7, lines 44-47.)

Securing/Means for securing a sync for examining only the fixed pattern (Referring to Figures 2 and 3, during synchronization the synchronization pattern is inherently examined individually in order to determine the value of each bit.)

Wherein step (a) processes the data until the sync is secured and step (b) processes the data after the sync is secured (Referring to Figures 2-4, when correctly detecting contiguous synchronization patterns, the frame number decoder **31** detects a sync frame number equal to the count value of the frame counter **32** and controls the frame counter **32** so as to output a frame number based on the detected number. See column 7, lines 61-65.)

6. Claims 1, 3-6, 12-15, 25-30, and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al. (US 5,289,476), hereinafter referred to as Johnson.

Regarding claims 1, 14, 25, 26, and 34 (respectively), Johnson discloses transmission mode detection in a modulated communication system, which comprises:

Generating/Means for generating a fixed pattern comprising 'm' words (Referring to Figure 6A, bit sync **610** comprised of 8-bits.)

Generating/Means for generating variable, non-random patterns of predetermined bit structure, each pattern comprising 'n' words, wherein the variable patterns are two patterns (Referring to Figure 6A, word sync **611** comprised of 7-bits representing one of two states, either BPSK or QPSK. See column 10, lines 13-15.)

Generating/Means for generating sync patterns comprising 'q' words, each of the sync patterns formed by combining the fixed pattern and one of the variable patterns (Referring to Figure 6A, the preamble comprises bit sync **610** and word sync **611**.)

Wherein the variable pattern comprises a plurality of words, and the variable patterns are made by changing an order of the words (Referring to Figure 6A, word sync **611** comprised of 7-bits representing one of two states, either BPSK or QPSK. See column 10, lines 13-15.)

Johnson does not disclose *adding one of said sync patterns to each of said data packets in a data stream, wherein consecutive ones of said data packets each have added respectively different variable patterns.*

However, Johnson teaches that the transmitter sends data packets using either BPSK or QPSK on a packet-by-packet basis by generating the appropriate word sync pattern for each

packet, thereby, making a bit structure in which includes different word syncs (See column 10, lines 18-21.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement BPSK and QPSK in consecutive packets resulting in a different sync patterns in the system of Johnson. One of ordinary skill in the art would have been motivated to do so in order to robustly transmit communication signals during noisy periods (BPSK) followed by higher data transmission during a consecutive period of lower impairment (QPSK) in an alternating style as taught by Johnson (See column 1, lines 40-45.)

Regarding claims 3 and 27 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Johnson does not disclose *wherein the fixed pattern comprises three words.*

Johnson teaches bit sync **610** comprised of 8-bits (See Figure 6A.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement additional bits in the bit sync preamble data packet of Johnson. One of ordinary skill in the art would have been motivated to do so in order to provide synchronization in highly congested and interference prone areas.

Regarding claims 4 and 28 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Johnson does not disclose *wherein the three words include 'eb', 'cb' and 'aa', expressed in a hexadecimal notation.*

Johnson teaches a word sync **611** comprised of 7-bits representing one of two states, either BPSK or QPSK (See column 10, lines 13-15.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine three different fixed patterns in the synchronization preamble of Johnson. One of ordinary skill in the art would have been motivated to do so in order to provide synchronization in highly congested and interference prone areas.

Regarding claims 5 and 29 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Johnson does not disclose *wherein the variable pattern comprises five words.*

Johnson teaches a word sync **611** comprised of 7-bits representing one of two states, either BPSK or QPSK (See column 10, lines 13-15.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to increase the length of the word sync to comprise five words. One of ordinary skill in the art would have been motivated to so in order to provide synchronization in highly congested and interference prone areas.

Regarding claims 6 and 30 as explained in the rejection statements of claims 1 and 25, Fujimoto discloses all of the claim limitations of claims 1 and 25 (parent claims).

Johnson does not disclose *wherein the five words include '4c', 'ea', 'cd', '7a' and '81', expressed in a hexadecimal notation.*

Johnson teaches a word sync **611** comprised of 7-bits representing one of two states, either BPSK or QPSK (See column 10, lines 13-15.)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine five different fixed patterns in the synchronization preamble of Johnson.

One of ordinary skill in the art would have been motivated to do so in order to provide synchronization in highly congested and interference prone areas.

Regarding claims 12 and 32, the primary reference further teaches *the method including a step of detecting a sync* (Referring to Figure 2, the preamble is detected to identify the beginning of a data packet. See column 7, lines 58-61.)

Regarding claims 13, 15, 33, and 35, the primary reference further teaches comprising:

Detecting/Means for detecting a sync for examining both of a fixed pattern and a variable pattern of a data received (Referring to Figure 2, the preamble is detected to identify the beginning of a data packet, the preamble comprises the bit sync and word sync. See column 7, lines 58-61.)

Securing/Means for securing a sync for examining only the fixed pattern (Referring to Figure 2, during synchronization the bit sync is inherently examined individually in order to determine the value of each bit.)

Wherein step (a) processes the data until the sync is secured and step (b) processes the data after the sync is secured (Referring to Figures 2 and 6A, the preamble detector process the data packet while determining synchronization and then process the data packet. See column 7, lines 58-61.)

Allowable Subject Matter

7. Claims 6, 7, 31, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 17-24 are allowed.

Response to Arguments

9. Applicant's arguments filed 21 September 2006 have been fully considered but they are not persuasive.

Rejection Under 35 USC 102

On page 13 of the remarks, regarding claims 1 and 14, the Applicant argues Fujimoto does not disclose *wherein the variable patterns comprise a plurality of words, and the variable patterns are made by changing an order of the words.* The Examiner respectfully disagrees. Note: the Examiner interprets a single bit as a "word." With this interpretation in mind, Fujimoto discloses synchronization patterns **SY0** to **SY7** are assigned logical patterns of data comprising a variable portion, with different bit patterns, comprised of different composite patterns (See column 5, lines 33-38.) Therefore, Fujimoto discloses *wherein the variable pattern comprises a plurality of words, and the variable patterns are made by changing an order of the words.*

Rejection Under 35 USC 103

On page 15 of the remarks, regarding claims 1 and 14, the Applicant argues Johnson does not teach *wherein the variable patterns comprise a plurality of words, and the variable patterns are made by changing an order of the words.* The Examiner respectfully disagrees. Note: the Examiner interprets a single bit as a "word." With this interpretation in mind, Johnson teaches a word sync **611** comprised of 7-bits representing one of two states, either BPSK or QPSK (See

column 10, lines 13-15.) Therefore, Johnson teaches *wherein the variable patterns comprise a plurality of words, and the variable patterns are made by changing an order of the words.*

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald L. Mills whose telephone number is 571-272-3094. The examiner can normally be reached on 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donald L Mills

DLM

October 18, 2006

Seema S. Rao 10/26/06

SEEMA S. RAO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600